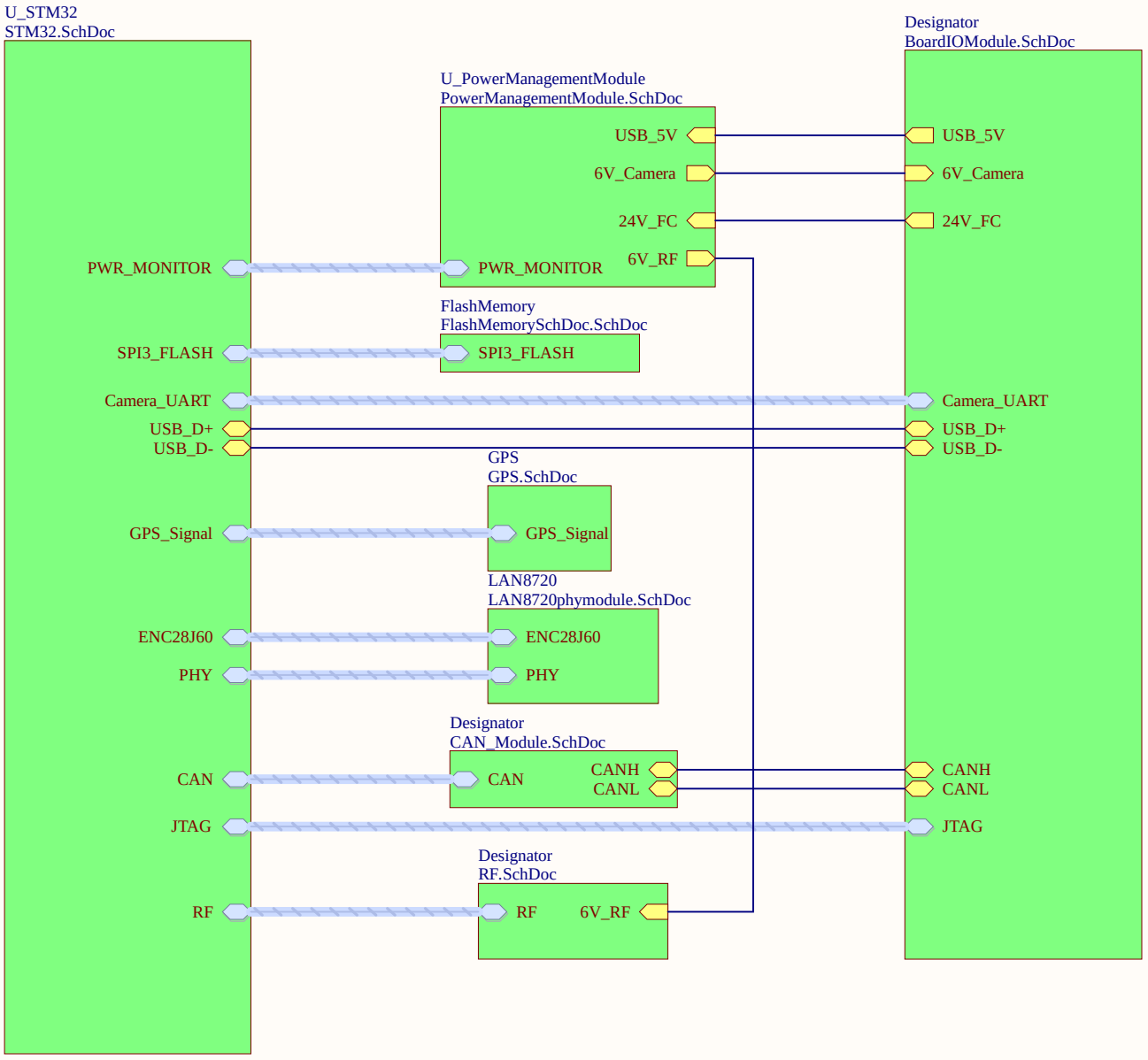
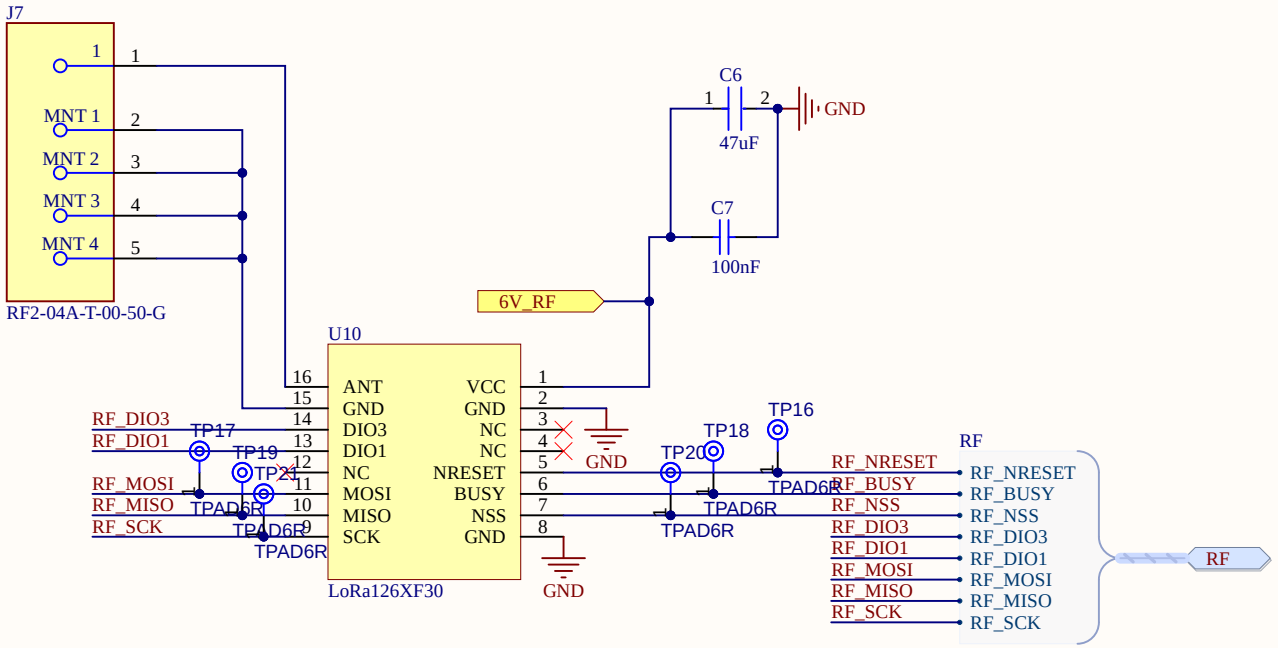
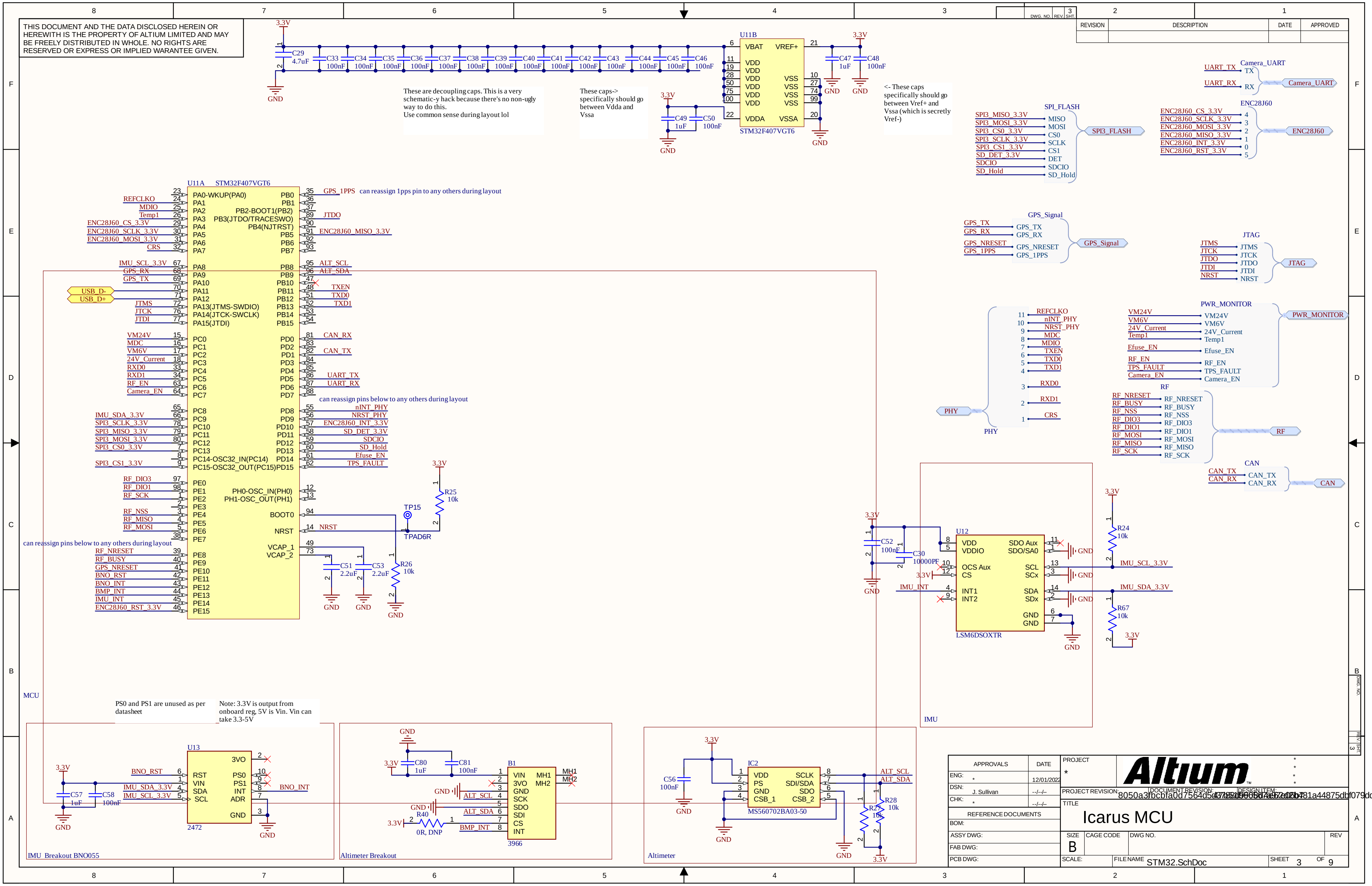


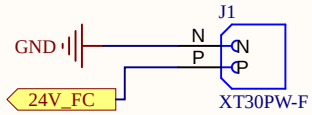
BURPG		PROJECT	ArgoTele.PrjPcb
APPROVALS	DATE	SIZE	Title / REV
Drawn: J. Sullivan	07/28/22	A	Icarus Flight Computer
Approved: *	--/--/--	SCALE:	FILE NAME TopSheet.SchDoc — SHEET 1 OF 9



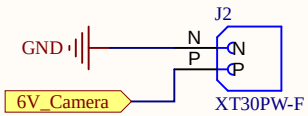
Title		
Size A	Number	Revision
Date: 6/16/2026		Sheet of
File: C:\Users\..\RF.SchDoc		Drawn By:


THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.
These are decoupling caps. This is a very schematic-y hack because there's no non-ugly way to do this. Use common sense during layout lol
These caps-> specifically should go between Vdda and Vssa
<- These caps specifically should go between Vref+ and Vssa (which is secretly Vref-)
U11B STM32F407VGT6
U11A STM32F407VGT6
can reassign 1pps pin to any others during layout
can reassign pins below to any others during layout
can reassign pins below to any others during layout
SPI_FLASH
ENC28J60
Camera_UART
GPS_Signal
JTAG
PWR_MONITOR
PHY
RF
CAN
U12 LSM6DSOXTR
IMU
MCU
PS0 and PS1 are unused as per datasheet
Note: 3.3V is output from onboard reg, 5V is Vin. Vin can take 3.3-5V
U13 2472
IMU_Breakout BNO055
B1 3966
Altimeter Breakout
IC2 MS560702BA03-50
Altimeter
APPROVALS
DATE
ENG:
DSN: J. Sullivan
CHK:
12/01/2022
REFERENCE DOCUMENTS
BOM:
ASSY DWG:
FAB DWG:
PCB DWG:
PROJECT
Altium
TITLE
Icarus MCU
SIZE B
CAGE CODE
DWG NO.
REV
SCALE:
FILE NAME STM32.SchDoc
SHEET 3 OF 9
REVISION
DESCRIPTION
DATE
APPROVED

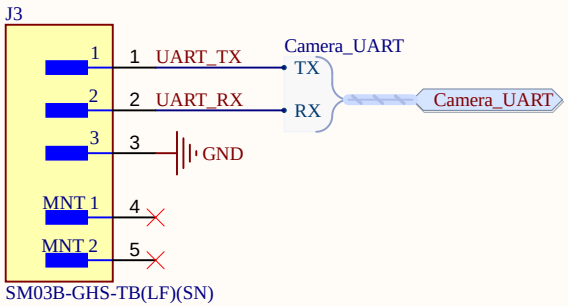
Someone should check Polarity here LOL



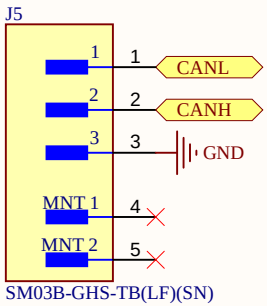
FC Power Input



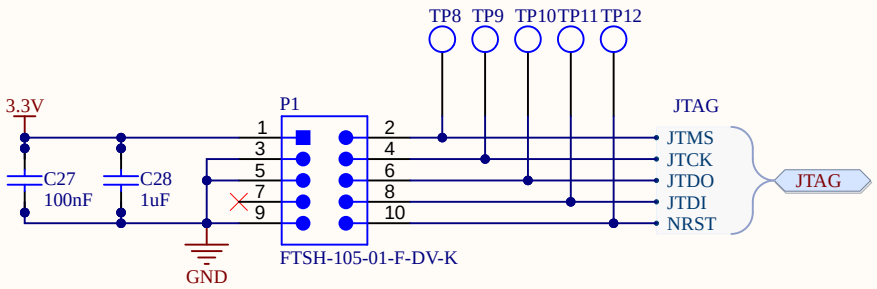
Camera Power Output



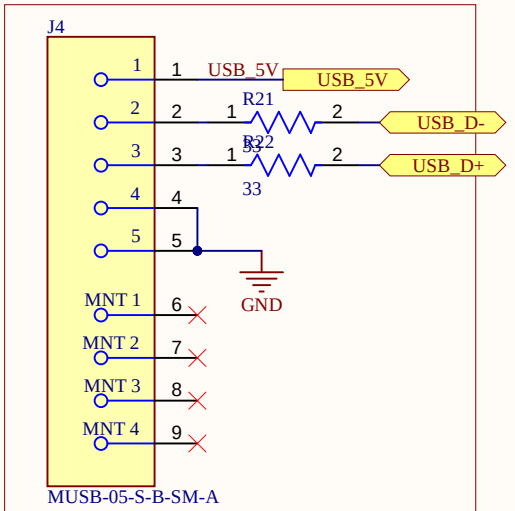
UART Connector



CAN Connector



JTAG



USB

Peripheral Connector

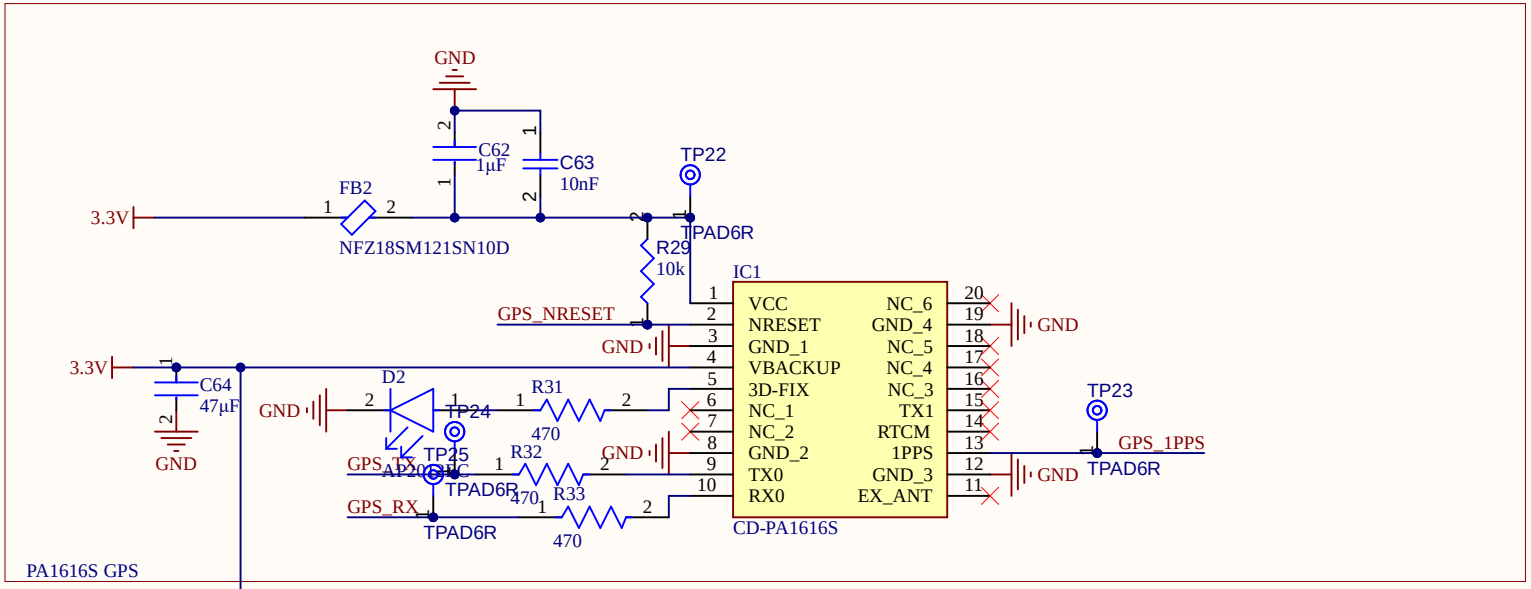
BURPG

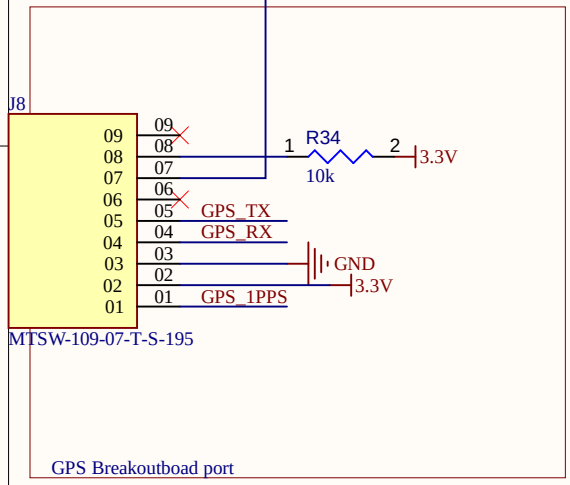
APPROVALS	DATE
Drawn: J. Sullivan	7/26/22
Approved: *	

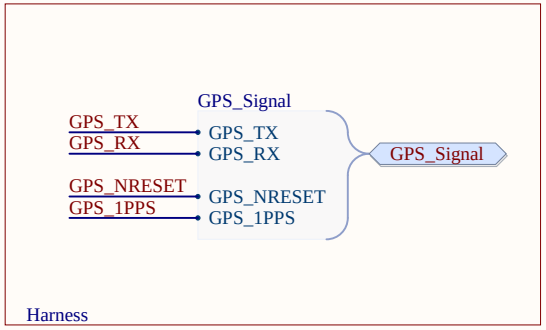
PROJECT: ArgoTele.PrjPcb

SIZE	Title	REV
A	Board IO/Connectors Module	

SCALE: | FILE NAME: BoardIOModule.SchDoc | SHEET 4 OF 9







Title		
Size A	Number	Revision
Date: 6/16/2026		Sheet of
File: C:\Users\..\GPS.SchDoc		Drawn By:

REVISION	DESCRIPTION	DATE	APPROVED

place these as close to LAN8720 as possible

check which one is green and which is yellow when doing layout, swap pullups/pulldowns accordingly

place this 0ohm close to magnetics

Create EGND copper pour around Rj45

ENC28J60 Ethernet MAC+PHY

APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

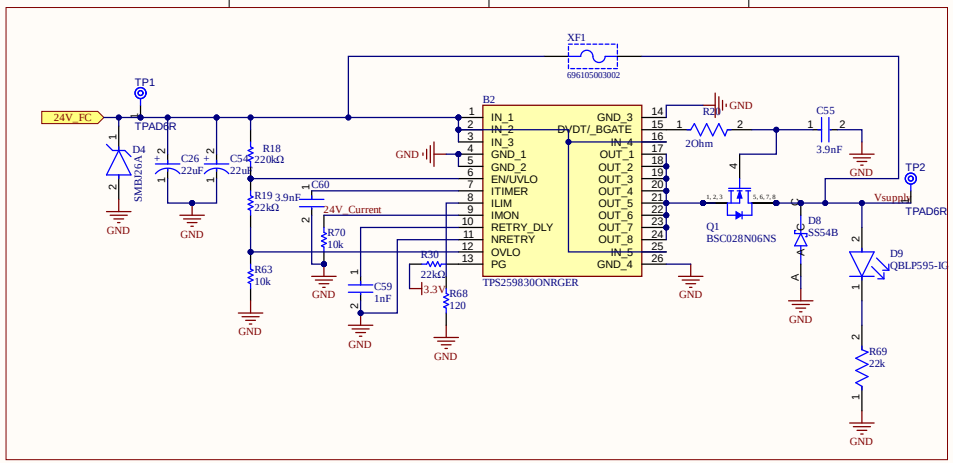
PROJECT: Altium

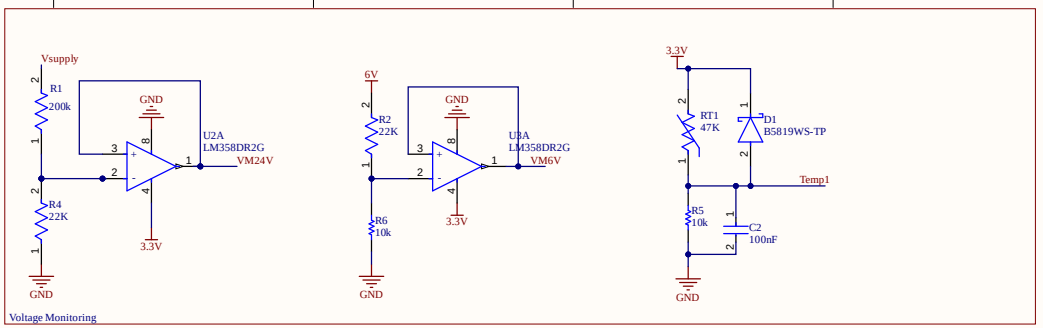
PROJECT REVISION: 8050a3fbcbfa0d7564d5c [illegible] 37f790c77b39e0a

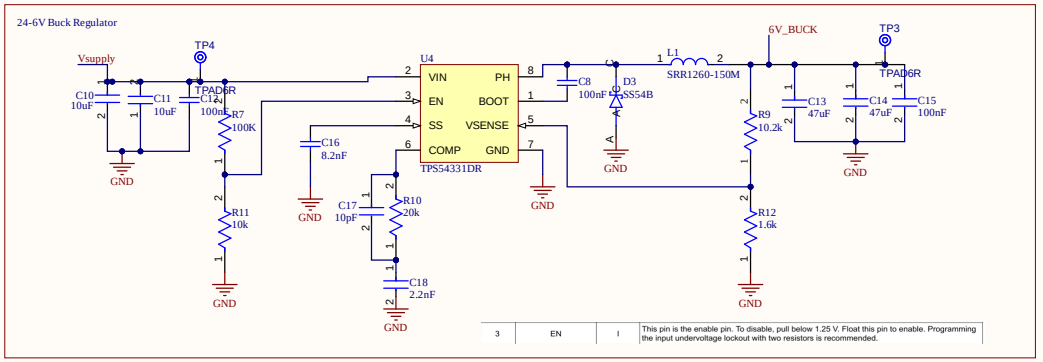
TITLE: *

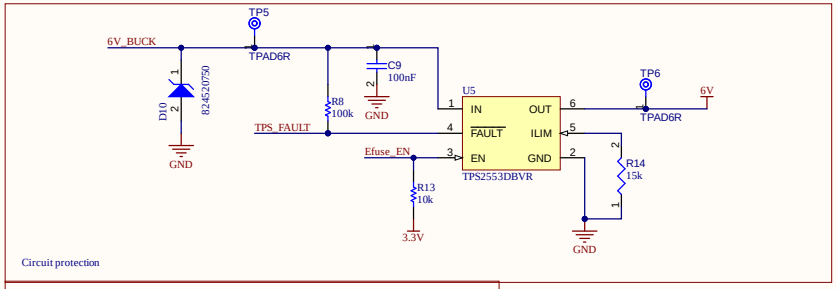
SIZE	CAGE CODE	DWG NO.	REV
B			

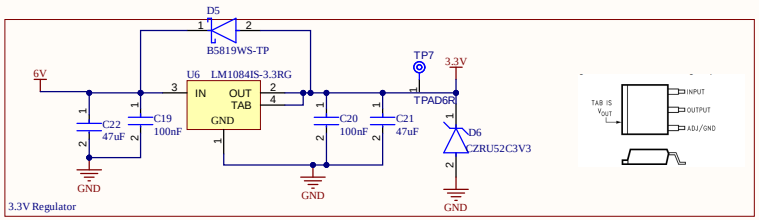
SCALE: | FILE NAME: LAN8720phymodule.SchDoc | SHEET 6 OF 9

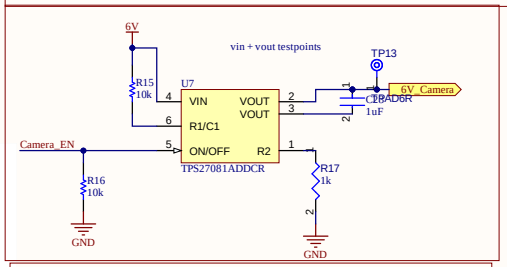


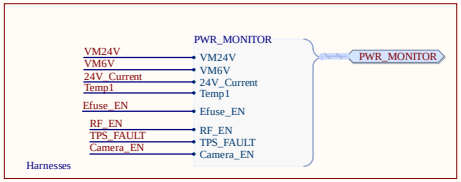


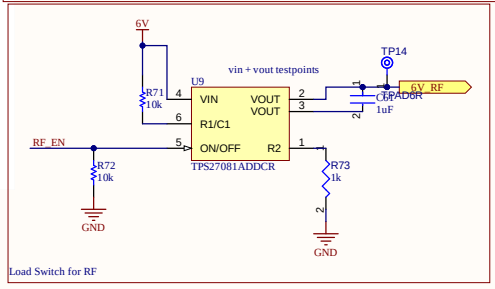


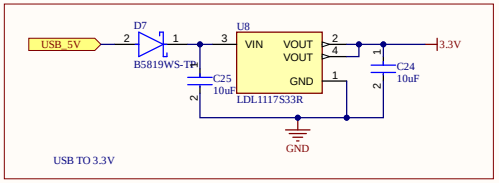












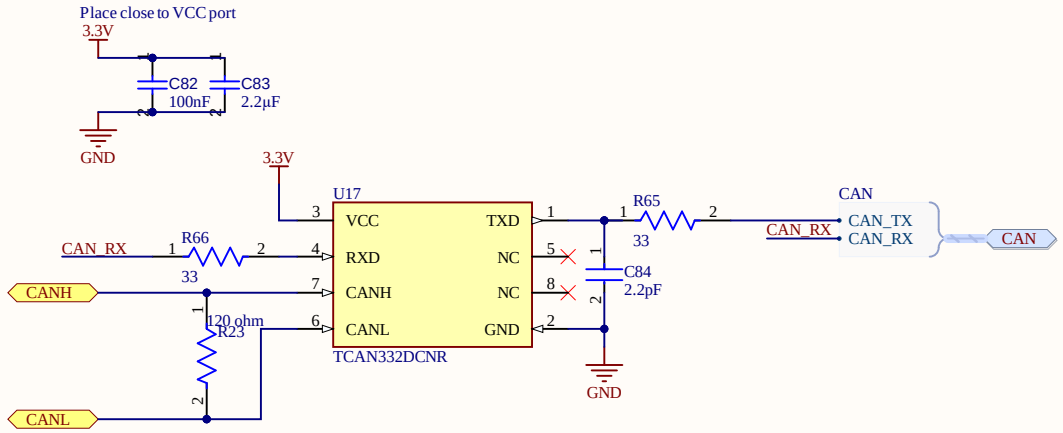
Load Switch for Camera

BURPG	PROJECT: ArgoTele.PrjPcb		
APPROVALS	DATE	SIZE: A	Title: Icarus Power Management Module
Drawn: J. Sullivan	7/28/22		
Approved: *	*	SCALE:	FILENAME: PowerManagementModule.SchDoc SHEET 7 OF 9

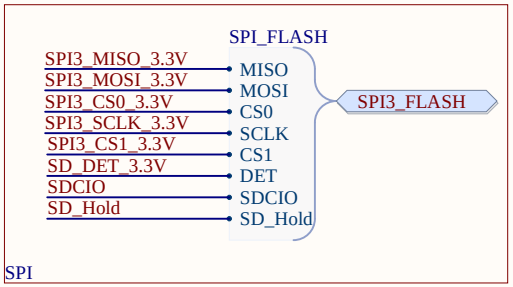
6.1 Absolute Maximum Ratings

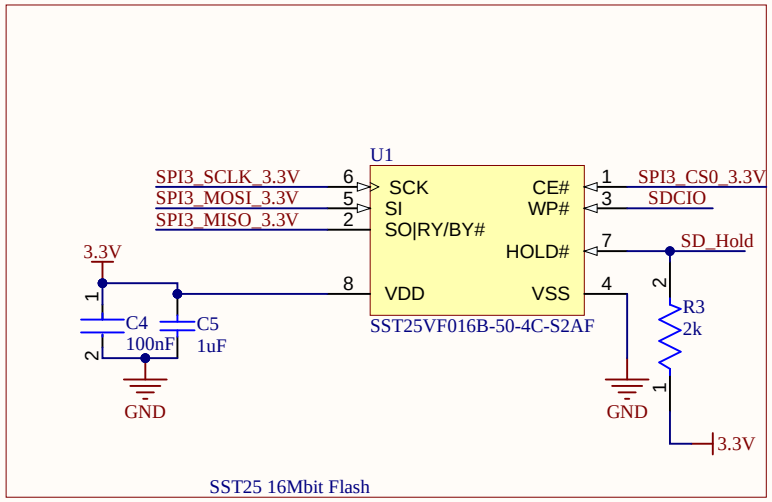
over operating free-air temperature range (unless otherwise noted) (1)

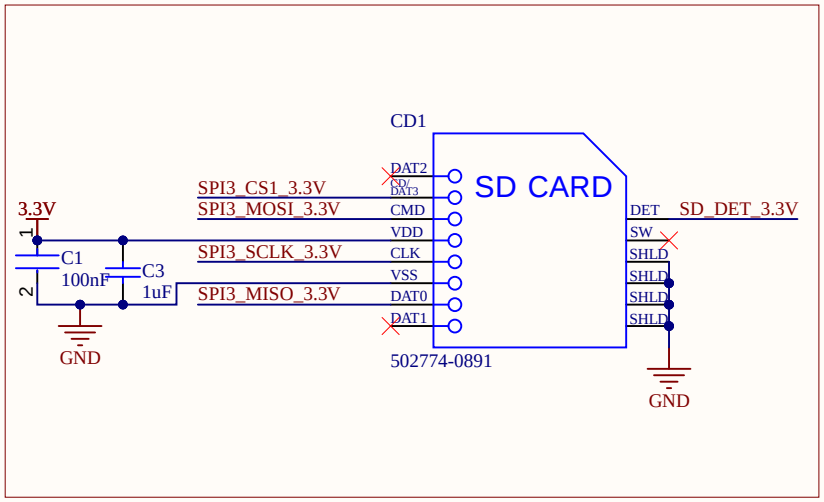
		MIN	MAX	UNIT
Input voltage	VIN	–0.3	30	V
	EN	–0.3	6	
	BOOT		38	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	SS	–0.3	3	



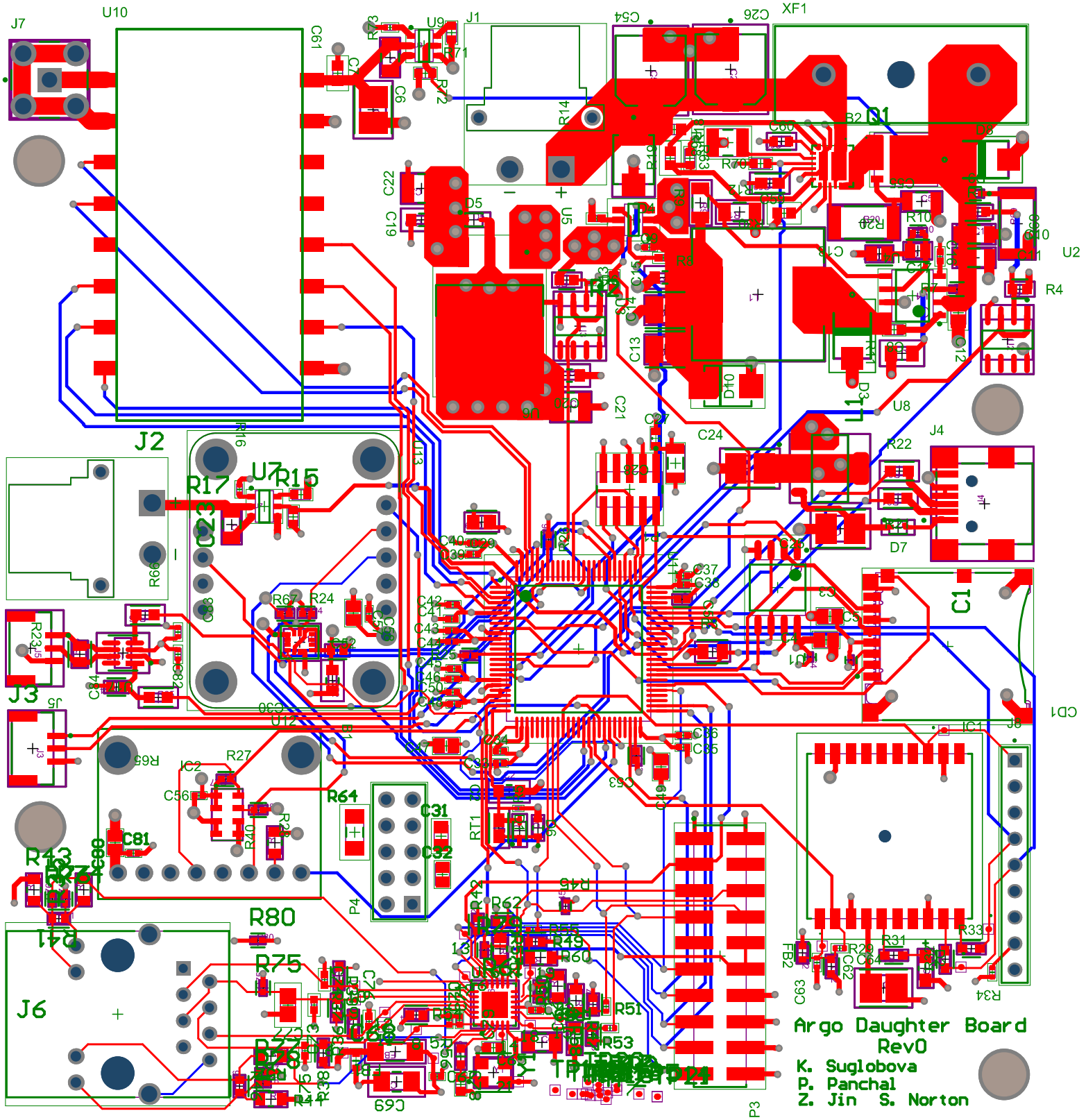
Title		
Size: A4	Number	Revision
Date: 6/16/2026		Sheet of
File: C:\Users\..\CAN_Module.SchDoc		Drawn By:







BURPG		PROJECT	ArgoTele.PrjPcb	
APPROVALS	DATE	SIZE	Title	REV
Drawn: *		A	*	
Approved: *		SCALE:	FILE NAME FlashMemorySchDoc.SchDoc	SHEET 9 OF 9


Argo Daughter Board
RevO
K. Suglobova
P. Panchal
Z. Jin S. Norton